Amendment to Claims

1 (currently amended). A method for manufacturing an integrated circuit comprising a nonvolatile memory, the method comprising:

forming a first structure over a semiconductor substrate, the first structure comprising:

a first conductive gate of a nonvolatile memory cell; and

a first dielectric over the first conductive gate;

forming a layer ("FG layer") to provide at least two conductive floating gates for the memory cell, wherein each floating gate comprises a first portion and an upward protruding second portion, the second portion being formed over the first dielectric and overlaying a sidewall of the first conductive gate;

wherein the memory cell comprises two source/drain regions and a channel region which borders on the source/drain regions, and each floating gate of the memory cell is operable to control a portion of the channel region.

2 (currently amended). ~~The method of Claim 1~~

A method for manufacturing an integrated circuit comprising a nonvolatile memory, the method comprising:

forming a first structure over a semiconductor substrate, the first structure comprising:

a first conductive gate of a nonvolatile memory cell; and

a first dielectric over the first conductive gate;

forming a layer ("FG layer") to provide at least two conductive floating gates for the memory cell, wherein each floating gate comprises a first portion and an upward protruding

second portion, the second portion being formed over the first dielectric and overlaying a sidewall of the first conductive gate;

wherein the FG layer comprises a first sub-layer and a second sub-layer formed after the first sub-layer, wherein the first portion of each floating gate is formed from the first sub-layer, and the second portion of each floating gate is formed from the second sub-layer.

3 (original). The method of Claim 2 wherein forming the FG layer comprises:

forming the first sub-layer to provide the first portions of the floating gates, the first structure protruding above the first sub-layer; and then

forming the second sub-layer layer and etching the second sub-layer to provide the second portions of the floating gates on sidewalls of the first structure.

4 (original). The method of Claim 1 wherein the FG layer consists of one or more sub-layers all of which are present in both the first and the second portions of the floating gates.

5 (currently amended). ~~The method of Claim 4~~

A method for manufacturing an integrated circuit comprising a nonvolatile memory, the method comprising:

forming a first structure over a semiconductor substrate, the first structure comprising:

a first conductive gate of a nonvolatile memory cell; and

a first dielectric over the first conductive gate;

forming a layer ("FG layer") to provide at least two conductive floating gates for the memory cell, wherein each floating gate comprises a first portion and an upward protruding

second portion, the second portion being formed over the first dielectric and overlaying a sidewall of the first conductive gate;

wherein the FG layer consists of one or more sub-layers all of which are present in both the first and the second portions of the floating gates;

wherein forming the FG layer comprises:

forming the FG layer over the first structure; and then

etching the FG layer anisotropically without a mask over the memory cell to remove the FG layer from over the top of the first structure but leave the FG layer over the first dielectric over the sidewall of the first structure.

6 (original). The method of Claim 5 further comprising forming substrate isolation regions, each substrate isolation region being a dielectric region having a portion protruding above the semiconductor substrate;

wherein forming the FG layer over the first structure results in the FG layer having a greater thickness between the substrate isolation regions next to the first structure than over the substrate isolation regions;

wherein etching the FG layer results in the FG layer being etched off from over at least portions of the substrate isolation regions and the first structure but not between the substrate isolation regions next to the first structure.

7 (original). The method of Claim 1 wherein the memory cell is one of a plurality of the memory cells, and the method further comprises a masked etch of the FG layer to remove portions of the FG layer between different memory cells.

8 (original). The method of Claim 1 further comprising forming two second conductive gates for the memory cell, the second conductive gates being insulated from the first conductive gate and the floating gates.

9 (currently amended). ~~The method of Claim 8~~

A method for manufacturing an integrated circuit comprising a nonvolatile memory, the method comprising:

forming a first structure over a semiconductor substrate, the first structure comprising:

a first conductive gate of a nonvolatile memory cell; and

a first dielectric over the first conductive gate;

forming a layer ("FG layer") to provide at least two conductive floating gates for the memory cell, wherein each floating gate comprises a first portion and an upward protruding second portion, the second portion being formed over the first dielectric and overlaying a sidewall of the first conductive gate;

forming two second conductive gates for the memory cell, the second conductive gates being insulated from the first conductive gate and the floating gates.

wherein forming the FG layer to provide the floating gates comprises:

forming the FG layer;

forming a dielectric D1 over the FG layer;

forming a layer G2 over the dielectric D1, wherein each second conductive gate comprises a portion of the layer G2, wherein the layer G2 has a portion P1 protruding above the first conductive gate;

forming a layer L1 over the layer G2 such that the protruding portion P1 is exposed and not completely covered by the layer L1;

at least partially removing the protruding portion P1 to form a through hole in the layer G2 over the first conductive gate, wherein at a conclusion of this removing operation a portion of the layer G2 remains covered by the layer L1;

forming a layer L2 on the layer G2 adjacent to the through hole; and

removing at least parts of the layers L1 and G2 and of the FG layer selectively to the layer L2.

10-19 (canceled).

20 (new). The method of Claim 8 wherein each floating gate in combination with a respective one of the second conductive gates is operable to control a respective portion of the channel region.

21 (new). The method of Claim 1 wherein the at least two floating gates are operable to control respective first and second portions of the channel region, and the first conductive gate is operable to control a third portion of the channel region.

22 (new). The method of Claim 1 wherein the first conductive gate is formed before the FG layer.

23 (new). The method of Claim 2 wherein the memory cell is one of a plurality of the memory cells, and the method further comprises a masked etch of the FG layer to remove portions of the FG layer between different memory cells.

24 (new). The method of Claim 2 further comprising forming two second conductive gates for the memory cell, the second conductive gates being insulated from the first conductive gate and the floating gates.

25 (new). The method of Claim 2 wherein the memory cell comprises two source/drain regions and a channel region which borders on the source/drain regions, and each floating gate of the memory cell is operable to control a portion of the channel region.

26 (new). The method of Claim 2 further comprising forming two second conductive gates for the memory cell, the second conductive gates being insulated from the first conductive gate and the floating gates, wherein the memory cell comprises two source/drain regions and a channel region which borders on the source/drain regions, and each floating gate in combination with a respective one of the second conductive gates is operable to control a respective portion of the channel region.

27 (new). The method of Claim 26 wherein the first conductive gate is operable to control a portion of the channel region between said two respective portions of the channel region.

28 (new). The method of Claim 2 wherein the memory cell comprises two source/drain regions and a channel region which borders on the source/drain regions, and each floating gate of the memory cell overlies a portion of the channel region.

29 (new). The method of Claim 2 wherein the second portions of at least two floating gates overlay respective two opposite sidewalls of the first conductive gate.

30 (new). The method of Claim 2 wherein the first conductive gate is formed before the FG layer.

31 (new). The method of Claim 5 wherein the memory cell is one of a plurality of the memory cells, and the method further comprises a masked etch of the FG layer to remove portions of the FG layer between different memory cells.

32 (new). The method of Claim 5 further comprising forming two second conductive gates for the memory cell, the second conductive gates being insulated from the first conductive gate and the floating gates.

33 (new). The method of Claim 5 wherein the memory cell comprises two source/drain regions and a channel region which borders on the source/drain regions, and each floating gate of the memory cell is operable to control a portion of the channel region.

34 (new). The method of Claim 5 further comprising forming two second conductive gates for the memory cell, the second conductive gates being insulated from the first conductive gate and the floating gates, wherein the memory cell comprises two source/drain regions and a channel region which borders on the source/drain regions, and each floating gate in combination with a respective one of the second conductive gates is operable to control a respective portion of the channel region.

35 (new). The method of Claim 34 wherein the first conductive gate is operable to control a portion of the channel region between said two respective portions of the channel region.

36 (new). The method of Claim 5 wherein the memory cell comprises two source/drain regions and a channel region which borders on the source/drain regions, and each floating gate of the memory cell overlies a portion of the channel region.

37 (new). The method of Claim 5 wherein the second portions of at least two floating gates overlay respective two opposite sidewalls of the first conductive gate.

38 (new). The method of Claim 9 wherein the memory cell is one of a plurality of the memory cells, and the method further comprises a masked etch of the FG layer to remove portions of the FG layer between different memory cells.

39 (new). The method of Claim 9 further comprising forming two second conductive gates for the memory cell, the second conductive gates being insulated from the first conductive gate and the floating gates.

40 (new). The method of Claim 9 wherein the memory cell comprises two source/drain regions and a channel region which borders on the source/drain regions, and each floating gate of the memory cell is operable to control a portion of the channel region.

41 (new). The method of Claim 9 further comprising forming two second conductive gates for the memory cell, the second conductive gates being insulated from the first conductive gate and the floating gates, wherein the memory cell comprises two source/drain regions and a channel region which borders on the source/drain regions, and each floating gate in combination with a respective one of the second conductive gates is operable to control a respective portion of the channel region.

42 (new). The method of Claim 41 wherein the first conductive gate is operable to control a portion of the channel region between said two respective portions of the channel region.

43 (new). The method of Claim 9 wherein the memory cell comprises two source/drain regions and a channel region which borders on the source/drain regions, and each floating gate of the memory cell overlies a portion of the channel region.

44 (new). The method of Claim 9 wherein the second portions of at least two floating gates overlay respective two opposite sidewalls of the first conductive gate.

45 (new). The method of Claim 9 wherein the first conductive gate is formed before the FG layer.

46 (new). A method for manufacturing an integrated circuit comprising a nonvolatile memory, the method comprising:

forming a first structure over a semiconductor substrate, the first structure comprising:

a first conductive gate of a nonvolatile memory cell; and

a first dielectric over the first conductive gate;

forming a layer ("FG layer") to provide at least two conductive floating gates for the memory cell, wherein each floating gate comprises a first portion and an upward protruding second portion, the second portion being formed over the first dielectric and overlaying a sidewall of the first conductive gate;

wherein the memory cell comprises two source/drain regions and a channel region which borders on the source/drain regions, and each floating gate of the memory cell overlies a portion of the channel region.

47 (new). The method of Claim 46 wherein the first conductive gate is formed before the FG layer.

48 (new). A method for manufacturing an integrated circuit comprising a nonvolatile memory, the method comprising:

forming a first structure over a semiconductor substrate, the first structure comprising:

a first conductive gate of a nonvolatile memory cell; and

a first dielectric over the first conductive gate;

forming a layer ("FG layer") to provide at least two conductive floating gates for the memory cell, wherein each floating gate comprises a first portion and an upward protruding second portion, the second portion being formed over the first dielectric and overlaying a sidewall of the first conductive gate;

wherein the second portions of at least two floating gates overlay respective two opposite sidewalls of the first conductive gate.

49 (new). The method of Claim 48 wherein the first conductive gate is formed before the FG layer.